AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Withdrawn) A method of fabricating a semiconductor integrated circuit device that has a standby current of 5 μA or below in tests of operation at 90°C and has MISFETs formed on the main surface of a semiconductor substrate, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode by patterning the silicon film deposited on said gate insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of said semiconductor substrate to 2.5 nm or less below the surface of said semiconductor substrate;

(e) forming a metal film on said source/drain regions;

(f) forming a metallic silicide layer where said source/drain regions are in contact with said metal film; and

(g) removing that part of said metal film which did not react in step (f).

2. (Cancelled)

3. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 1, wherein said sputter etching is carried out after the

surface of said semiconductor substrate has been cleaned by using hydrofluoric acid as a cleaning agent.

4. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 1, wherein said sputter etching is Ar sputter etching.

5. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 1, wherein said metal film is a film of Co.

6. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 1, wherein said MISFETs configure an SRAM memory cell.

7. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 1, wherein the metal forming step is performed, under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.

8. (Withdrawn) A method of fabricating a semiconductor integrated circuit device that has a standby current of 5 μA or below in tests of operation at 90°C and has MISFETs formed on the main surface of a semiconductor substrate, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode by patterning the silicon film deposited on said gate insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of said semiconductor substrate to 2.5 nm or less below the surface of said semiconductor substrate;

(e) forming a metal film on said source/drain regions and on said gate electrode;

(f) forming a metallic silicide layer where said source/drain regions are in contact with said metal film , and

(g) removing that part of said metal film which did not react in step (f).

9. (Cancelled)

10. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 8, wherein said sputter etching is carried out after the surface of said semiconductor substrate has been cleaned by using hydrofluoric acid as a cleaning agent.

11. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 8, wherein said sputter etching is Ar sputter etching.

12. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 8, wherein said metal film is a film of Co.

13. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 8, wherein said MISFETs configure an SRAM memory cell.

14. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 8, wherein the metal film forming step is performed, under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.

15. (Withdrawn) A method of fabricating a semiconductor integrated circuit device and has MISFETs formed on the main surface of a semiconductor substrate which has a standby current of 1 .5 μA or below in actual operation, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode by patterning the silicon film deposited on said gate insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of said semiconductor substrate to 2.5 nm or less below the surface of said semiconductor substrate;

(e) forming a metal film on said source/drain regions;

(f) forming a metallic silicide layer where said source/drain regions are in contact with said metal film; and

(g) removing that part of said metal film which did not react in step (f).

16. (Cancelled)

17. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 15, wherein said sputter etching is carried out after the surface of said semiconductor substrate has been cleaned by using hydrofluoric acid as a cleaning agent.

18. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 15, wherein said sputter etching is Ar sputter etching.

19. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 15, wherein said metal film is a film of Co.

20. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 15, wherein said MISFETs configure an SRAM memory cell.

21. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 15, wherein the metal forming step is performed, under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.

22. (Withdrawn) A method of fabricating a semiconductor integrated circuit device that has a standby current of 1 .5 μA or below in actual operation and has

MISFETs formed on the main surface of a semiconductor substrate, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode by patterning the silicon film deposited on said gate insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of said semiconductor substrate to 2.5 nm or less below the surface of said semiconductor substrate;

(e) forming a metal film on said source/drain regions and on said gate electrode;

(f) forming a metallic silicide layer where said source/drain regions are in contact with said metal film, and

(g) removing that part of said metal film which did not react in step (f).

23. (Cancelled)

24. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 22, wherein said sputter etching is carried out after the surface of said semiconductor substrate has been cleaned by using hydrofluoric acid as a cleaning agent.

25. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 22, wherein said sputter etching is Ar sputter etching.

26. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 22, wherein said metal film is a film of Co.

27. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 22, wherein said M1SFETs configure an SRAM memory cell.

28. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 22, wherein the metal film forming step is performed, under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.

29. (Withdrawn) A method of fabricating a semiconductor integrated circuit device that is battery-driven and has MISFETs formed on the main surface of a semiconductor substrate, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode by patterning the silicon film deposited on said gate insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of said semiconductor substrate to 2.5 nm or less below the surface of semiconductor substrate;

(e) forming a metal film on said source/drain regions;

(f) forming a metallic silicide layer where said source/drain regions are in contact with said metal film ; and

(g) removing that part of said metal film which did not react in step (f).

30. (Cancelled)

31. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 29, wherein said sputter etching is carried out after the surface of said semiconductor substrate has been cleaned by using hydrofluoric acid as a cleaning agent.

32. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 29, wherein said sputter etching is Ar sputter etching.

33. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 29, wherein said metal film is a film of Co.

34. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 29, wherein said MISFETs configure an SRAM memory cell.

35. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 29, wherein the metal film forming step is performed,

under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.

36. (Withdrawn) A method of fabricating a semiconductor integrated circuit device that is battery-driven and has MISFETs formed on the main surface of a semiconductor substrate, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode by patterning the silicon film deposited on said gate insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of semiconductor substrate to 2.5 nm or less below the surface of said semiconductor substrate;

(e) forming a metal film on said source/drain regions and on said gate electrode;

(f) forming a metallic silicide layer where said source/drain regions are in contact with said metal film , and

(g) removing that part of said metal film which did not react in step (f).

37. (Cancelled)

38. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 36, wherein said sputter etching is carried out after the

surface of said semiconductor substrate has been cleaned by using hydrofluoric acid as a cleaning agent.

39. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 36, wherein said sputter etching is Ar sputter etching.

40. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 36, wherein said metal film is a film of Co.

41. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 36, wherein said MISFETs configure an SRAM memory cell.

42. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 36, wherein the metal film forming step is performed, under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.

43. (Withdrawn) A method of fabricating a semiconductor integrated circuit device that has MISFETs formed on the main surface of a semiconductor substrate, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode with a width of 0.18 μm or less by patterning the silicon film that has been deposited on said gate-insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of said semiconductor substrate to 2.5 nm or less below the surface of said semiconductor substrate;

(e) forming a metal film on said source/drain regions;

(f) forming a metallic silicide layer with a thickness of 20 to 40 nm where said source/drain regions are in contact with said metallic film , and

(g) removing that part of said metal film which did not react in step (f).

44. (Cancelled)

45. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 43, wherein said sputter etching is carried out after the surface of said semiconductor substrate has been cleaned by using hydrofluoric acid as a cleaning agent.

46. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 43, wherein said sputter etching is Ar sputter etching.

47. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 43, wherein said metal film is a film of Co.

48. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 43, wherein said MISFETs configure an SRAM memory cell.

49. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 43, wherein the metal film forming step is performed, under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.

50. (Withdrawn) A method of fabricating a semiconductor integrated circuit device that is battery-driven and has MISFETs formed on the main surface of a semiconductor substrate, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode with a width of 0.18 pm or less by patterning the silicon film that has been deposited on said gate-insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of said semiconductor substrate and said gate electrode to 2.5 nm or less below the surface of said semiconductor substrate;

(e) forming a metal film on said source/drain regions and on said gate electrode;

(f) forming a metallic silicide layer with a thickness of 20 to 40 nm where said source/drain regions are in contact with said metallic film, and

(g) removing that part of said metal film which did not react in step (f).

51. (Cancelled)

52. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 50, wherein said sputter etching is carried out after the surface of said semiconductor substrate has been cleaned by using hydrofluoric acid as a cleaning agent.

53. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 50, wherein said sputter etching is Ar sputter etching.

54. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 50, wherein said metal film is a film of Co.

55. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 50, wherein said MISFETs configure an SRAM memory cell.

56. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 50, wherein the a metal film forming step is performed, under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.

57. (Withdrawn) A method of fabricating a semiconductor integrated circuit device that has MISFETs formed on the main surface of a semiconductor substrate, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode with a width of 0.18 μm or less by patterning the silicon film that has been deposited on said gate-insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of said semiconductor substrate to 2.5 nm or less below the surface of said semiconductor substrate;

(e) forming a metal film on said source/drain regions;

(f) forming a metallic suicide layer with sheet resistance of 5Ω□ to 12Ω□, where said source/drain regions are in contact with said metal film, and

(g) removing that part of said metal film which did not react in step (f).

58. (Cancelled)

59. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 57, wherein said sputter etching is carried out after the surface of said semiconductor substrate has been cleaned by using hydrofluoric acid as a cleaning agent.

60. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 57, wherein said sputter etching is Ar sputter etching.

61. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 57, wherein said metal film is a film of Co.

62. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 57, wherein said MISFETs configure an SRAM memory cell.

63. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 57, wherein the metal film forming step is performed, under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.

64. (Withdrawn) A method of fabricating a semiconductor integrated circuit device that is battery-driven and has MISFETs formed on the main surface of a semiconductor substrate, comprising the steps of:

(a) forming a gate-insulating film on said semiconductor substrate;

(b) forming a gate electrode with a width of 0.18 μm or less by patterning the silicon film that has been deposited on said gate-insulating film;

(c) forming the source/drain regions on both sides of said gate electrode by injecting impurities into the semiconductor substrate;

(d) sputter-etching away the top of said semiconductor substrate and on said gate electrode to 2.5 nm or less below the surface of said semiconductor substrate;

(e) forming a metal film on said source/drain regions and on said gate electrode;

(f) forming a metallic silicide layer with sheet resistance of 5Ω□ to 12Ω□, where said source/drain regions are in contact with said metal film, and

(g) removing that part of said metal film which did not react in step (f).

65. (Cancelled)

66. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 64, wherein said sputter etching is carried out after the surface of said semiconductor substrate has been cleaned by using hydrofluoric acid as a cleaning agent.

67. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 64, wherein said sputter etching is Ar sputter etching.

68. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 64, wherein said metal film is a film of Co.

69. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 64, wherein said MISFETs configure an SRAM memory cell.

70. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 64, wherein the metal film forming step is performed, under near-vacuum conditions, in the same apparatus in which said sputter etching has been carried out.

71. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 1, wherein said source/drain regions formed on both sides of the gate electrode include first source/drain regions, and wherein the method includes the further steps, between steps (c) and (d), of:

(c_1) forming side walls on side surfaces of said gate electrode; and

(c_2) forming second source/drain regions at sides of the side walls by injecting impurities into the semiconductor substrate, wherein said second source/drain regions have a higher impurity concentration than that of the first source/drain regions, and wherein said metal film is formed on said second source/drain regions.

72. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as claimed in claim 71, wherein said metal film is formed in contact with said second source/drain regions and not in contact with said first source/drain regions.

73. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 72, wherein said metallic silicide layer is positioned such that current leakage between said metallic suicide layer and a junction formed by said first source/drain regions and said semiconductor substrate is prevented.

74. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 1, wherein said metallic suicide layer has a thickness of 20 to 40 nm.

75. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 74, wherein said metal film is a cobalt film.

76. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 8, wherein said source/drain regions formed on both sides of the gate electrode include first source/drain regions, and wherein the method includes the further steps, between steps (c) and (d), of:

(c_1) forming side walls on side surfaces of said gate electrode; and

(c_2) forming second source/drain regions at sides of the side walls by injecting impurities into the semiconductor substrate, wherein said second source/drain regions have a higher impurity concentration than that of the first source/drain regions, and wherein said metal film is formed on said second source/drain regions.

77. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as claimed in claim 76, wherein said metal film is formed in contact with said second source/drain regions and not in contact with said first source/drain regions.

78. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 77, wherein said metallic silicide layer is positioned such

that current leakage between said metallic silicide layer and a junction formed by said first source/drain regions and said semiconductor substrate is prevented.

79. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 15, wherein said source/drain regions formed on both sides of the gate electrode include first source/drain regions, and wherein the method includes the further steps, between steps (c) and (d), of:

(c_1) forming side walls on side surfaces of said gate electrode; and

(c_2) forming second source/drain regions at sides of the side walls by injecting impurities into the semiconductor substrate, wherein said second source/drain regions have a higher impurity concentration than that of the first source/drain regions, and wherein said metal film is formed on said second source/drain regions.

80. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as claimed in claim 79, wherein said metal film is formed in contact with said second source/drain regions and not in contact with said first source/drain regions.

81. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 80, wherein said metallic silicide layer is positioned such that current leakage between said metallic silicide layer and a junction formed by said first source/drain regions and said semiconductor substrate is prevented.

82. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 22, wherein said source/drain regions formed on both sides of the gate electrode include first source/drain regions, and wherein the method includes the further steps, between steps (c) and (d), of:

(c_1) forming side walls on side surfaces of said gate electrode; and

(c_2) forming second source/drain regions at sides of the side walls by injecting impurities into the semiconductor substrate, wherein said second source/drain regions have a higher impurity concentration than that of the first source/drain regions, and wherein said metal film is formed on said second source/drain regions.

83. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as claimed in claim 82, wherein said metal film is formed in contact with said second source/drain regions and not in contact with said first source/drain regions.

84. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 83, wherein said metallic suicide layer is positioned such that current leakage between said metallic silicide layer and a junction formed by said first source/drain regions and said semiconductor substrate is prevented.

85. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 29, wherein said source/drain regions formed on both sides of the gate electrode include first source/drain regions, and wherein the method includes the further steps, between steps (c) and (d), of:

(c_1) forming side walls on side surfaces of said gate electrode; and

(c_2) forming second source/drain regions at sides of the side walls by injecting impurities into the semiconductor substrate, wherein said second source/drain regions have a higher impurity concentration than that of the first source/drain regions, and wherein said metal film is formed on said second source/drain regions.

86. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as claimed in claim 85, wherein said metal film is formed in contact with said second source/drain regions and not in contact with said first source/drain regions.

87. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 86, wherein said metallic silicide layer is positioned such that current leakage between said metallic suicide layer and a junction formed by said first source/drain regions and said semiconductor substrate is prevented.

88. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 36, wherein said source/drain regions formed on both sides of the gate electrode include first source/drain regions, and wherein the method includes the further steps, between steps (c) and (d), of:

(c_1) forming side walls on side surfaces of said gate electrode; and

(c_2) forming second source/drain regions at sides of the side walls by injecting impurities into the semiconductor substrate, wherein said second source/drain regions have a higher impurity concentration than that of the first

source/drain regions, and wherein said metal film is formed on said second source/drain regions.

89. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as claimed in claim 88, wherein said metal film is formed in contact with said second source/drain regions and not in contact with said first source/drain regions.

90. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 89, wherein said metallic suicide layer is positioned such that current leakage between said metallic silicide layer and a junction formed by said first source/drain regions and said semiconductor substrate is prevented.

91. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 43, wherein said source/drain regions formed on both sides of the gate electrode include first source/drain regions, and wherein the method includes the further steps, between steps (c) and (d), of:

(c_1) forming side walls on side surfaces of said gate electrode; and

(c_2) forming second source/drain regions at sides of the side walls by injecting impurities into the semiconductor substrate, wherein said second source/drain regions have a higher impurity concentration than that of the first source/drain regions, and wherein said metal film is formed on said second source/drain regions.

92. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as claimed in claim 91, wherein said metal film is formed in contact with said second source/drain regions and not in contact with said first source/drain regions.

93. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 92, wherein said metallic silicide layer is positioned such that current leakage between said metallic silicide layer and a junction formed by said first source/drain regions and said semiconductor substrate is prevented.

94. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 50, wherein said source/drain regions formed on both sides of the gate electrode include first source/drain regions, and wherein the method includes the further steps, between steps (c) and (d), of:

(c_1) forming side walls on side surfaces of said gate electrode; and

(c_2) forming second source/drain regions at sides of the side walls by injecting impurities into the semiconductor substrate, wherein said second source/drain regions have a higher impurity concentration than that of the first source/drain regions, and wherein said metal film is formed on said second source/drain regions.

95. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as claimed in claim 94, wherein said metal film is formed in contact with said second source/drain regions and not in contact with said first source/drain regions.

96. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 95, wherein said metallic suicide layer is positioned such that current leakage between said metallic silicide layer and a junction formed by said first source/drain regions and said semiconductor substrate is prevented.

97. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 57, wherein said source/drain regions formed on both sides of the gate electrode include first source/drain regions, and wherein the method includes the further steps, between steps (c) and (d), of:

(c_1) forming side walls on side surfaces of said gate electrode; and

(c_2) forming second source/drain regions at sides of the side walls by injecting impurities into the semiconductor substrate, wherein said second source/drain regions have a higher impurity concentration than that of the first source/drain regions, and wherein said metal film is formed on said second source/drain regions.

98. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as claimed in claim 97, wherein said metal film is formed in contact with said second source/drain regions and not in contact with said first source/drain regions.

99. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 98, wherein said metallic silicide layer is positioned such that current leakage between said metallic silicide layer and a junction formed by said first source/drain regions and said semiconductor substrate is prevented.

100. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 64, wherein said source/drain regions formed on both sides of the gate electrode include first source/drain regions, and wherein the method includes the further steps, between steps (c) and (d), of:

(c_1) forming side walls on side surfaces of said gate electrode; and

(c_2) forming second source/drain regions at sides of the side walls by injecting impurities into the semiconductor substrate, wherein said second source/drain regions have a higher impurity concentration than that of the first source/drain regions, and wherein said metal film is formed on said second source/drain regions.

101. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as claimed in claim 100, wherein said metal film is formed in contact with said second source/drain regions and not in contact with said first source/drain regions.

102. (Withdrawn) A method of fabricating a semiconductor integrated circuit device, as defined in claim 101, wherein said metallic silicide layer is positioned such that current leakage between said metallic silicide layer and a junction formed by said first source/drain regions and said semiconductor substrate is prevented.

103. (Currently Amended) A method of fabricating a semiconductor integrated circuit device, comprising the steps of:

(a) forming an isolating element in a semiconductor substrate;

(a)(b) forming ana first insulating film on athe semiconductor substrate;

(b)(c) forming a conductive film on said first insulating film and said isolating element, the conductive film having a width of 0.18 μm or less;

(c)(d) forming first semiconductor regions in said semiconductor substrate self-aligned with said conductive film;

(d)(e) forming second insulating films on side surfaces of said conductive film;

(e)(f) forming second semiconductor regions, having a greater impurity concentration than that of said first semiconductor regions, in said semiconductor substrate, self-aligned with said second insulating films;

(f)(g) removing the top of said semiconductor substrate to 2.5 nm or less below the surface of said semiconductor substrate by sputter-etching, and removing the top of said conductive film to 2.5 nm or less below the surface of the conductive film by sputter-etching; and

(g)(h) forming silicide layers in said surface of said semiconductor regions and said conductive film.

104. (Cancelled).

105. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 103, wherein said silicide layers are not in contact with said first semiconductor regions.

106. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 105, wherein said silicide layers are positioned such that current leakage between said suicide layers and junctions formed by the first semiconductor regions and said semiconductor substrate is prevented.

107. (Currently Amended) A method of fabricating a semiconductor integrated circuit device, as defined in claim 103, wherein said sputter etching is carried out after the surface of said semiconductor substrate ~~has~~and said conductive film have been cleaned by using hydrofluoric acid as a cleaning agent.

108. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 103, wherein said sputter etching is Ar sputter etching.

109. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 103, wherein said suicide layers are cobalt silicide layers.

110. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 109, wherein said cobalt silicide layers in the surface of said second semiconductor regions have a thickness of 20-40 nm.

111. (Cancelled)

112. (Currently Amended) A method of fabricating a semiconductor integrated circuit device, as defined in claim ~~111~~103, wherein the top of the conductive film is sputter-etched simultaneously with the sputter-etching away the top of said semiconductor substrate.

113. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 103, wherein the top of the semiconductor substrate is removed to a depth of 1 nm to 2.5 nm below the surface of said semiconductor substrate.

114. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 103, wherein the top of the semiconductor substrates is removed so as to form a recessed section of the semiconductor substrate.

115. (Currently Amended) A method of fabricating a semiconductor integrated circuit device, as defined in claim ~~111~~103, wherein the top of the conductive film is recessed by the sputter-etching thereof.

116. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 114, wherein the top of the semiconductor substrate is removed so as to form a recessed section of the semiconductor substrate.

117. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 103, wherein the depth of said first semiconductor region is 50 nm or less.

118. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 117, wherein the depth of said second semiconductor region is 150 nm or less.

119. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 117, wherein said sputter-etching is Ar sputter-etching.

120. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 117, wherein said silicide layers are cobalt silicide layers.

121. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 120, wherein said cobalt silicide layers in the surface of said second semiconductor regions have a thickness of 20-40 nm.

122. – 123. (Cancelled)

124. (Currently Amended) A method of fabricating a semiconductor integrated circuit device having a MISFET, comprising the steps of:

(a) forming an isolating element in a semiconductor substrate;

(~~a~~)(b) forming a gate insulating film of said MISFET on asaid semiconductor substrate;

(~~b~~)(c) forming a gate electrode of said MISFET on said gate insulating film and on said isolating element, said gate electrode having a width of 0.18 μm or less;

(~~c~~)(d) forming first source/drain regions of said MISFET in said semiconductor substrate self-aligned with said gate electrode, a depth of said first source/drain regions being 50 nm or less below the surface of said semiconductor substrate;

(~~d~~)(e) forming side walls of said MISFET on side surfaces of said gate electrode;

(~~e~~)(f) forming second source/drain regions of said MISFET, having a greater impurity concentration than that of said first source/drain regions, in said semiconductor substrate, self-aligned with said side walls, a depth of said second source/drain regions being 150 nm or less below the surface of said semiconductor substrate;

(f)(g) cleaning the surface of said semiconductor substrate and the surface of said gate electrode by using hydrofluoric acid as a cleaning agent;

(~~g~~)(h) removing the top of said second source/drain regions to 2.5 nm or less below the surface of said semiconductor substrate by sputter-etching, and removing the top of said gate electrode to 2.5 nm or less below the surface of the gate electrode by sputter-etching;

~~(h)~~(i) depositing a metal layer over ~~at least~~ said gate electrode, and first and second source/drain regions, wherein said steps ~~(g)~~(h) and ~~(h)~~(i) take place as sequential processes in a same apparatus; and

~~(i)~~(j) forming silicide layers in said surface of said second source/drain regions and said gate electrode by annealing said metal layer.

125. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 124, wherein said suicide layers are not in contact with said first semiconductor regions.

126. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 125, wherein said silicide layers are positioned such that current leakage between said silicide layers and junctions formed by the first source/drain regions and said semiconductor substrate is prevented.

127. (Currently Amended) A method of fabricating a semiconductor integrated circuit device having a MISFET, comprising the steps of:

(a) forming an isolating element in a semiconductor substrate;

~~(a)~~(b) forming a gate insulating film of said MISFET on ~~a~~ said semiconductor substrate;

~~(b)~~(c) forming a gate electrode of said MISFET on said gate insulating film and on said isolating element, a width of said gate electrode being 0.18 μm or less;

~~(c)~~(d) forming first source/drain regions of said MISFET in said semiconductor substrate self-aligned with sad gate electrode, a depth of said first source/drain regions being 50 nm or less below the surface of said semiconductor substrate;

~~(d)~~(e) forming side walls of said MISFET on side surfaces of said gate electrode;

~~(e)~~(f) forming second source/drain regions of said MISFET, having a greater impurity concentration than that of said first source/drain regions, in said semiconductor substrate, self-aligned with said side walls, a depth of said second source/drain regions being 150 nm or less below the surface of said semiconductor substrate;

~~(f)~~(g) removing the top of said second source/drain regions to 2.5 nm or less below the surface of said semiconductor substrate by sputter-etching, and removing the top of said gate electrode by 2.5 nm or less below the surface of said gate electrode by sputter-etching; and

~~(g)~~(h) forming silicide layers in said surface of said second source/drain regions and said gate electrode,

wherein said silicide layers are not in contact with junctions formed by said first source/drain regions and said semiconductor substrate, thereby a current leakage between said silicide layers and said junctions is prevented.

128. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 127, wherein said sputter-etching is Ar sputter-etching.

129. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 127, wherein said silicide layers are cobalt silicide layers.

130. (Previously Presented) A method of fabricating a semiconductor integrated circuit device, as defined in claim 129, wherein said cobalt silicide layers in the surface of said second semiconductor regions have a thickness of 20-40 nm.

131. (Cancelled)

132. (Currently Amended) A method of fabricating a semiconductor integrated circuit device, as defined in claim ~~131~~127, wherein the top of the gate electrode is sputter-etched.

133. (New) A method of fabricating a semiconductor integrated circuit device, as defined in claim 103,

wherein said step (a) comprises:

(a1) forming a trench in said semiconductor substrate; and

(a2) depositing a third insulating film in said trench.

134. (New) A method of fabricating a semiconductor integrated circuit device, as defined in claim 124,

wherein said step (a) comprises:

(a1) forming a trench in said semiconductor substrate; and

(a2) depositing an insulating film in said trench.

135. (New) A method of fabricating a semiconductor integrated circuit device, as defined in claim 127,

wherein said step (a) comprises:

(a1) forming a trench in said semiconductor substrate; and

(a2) depositing an insulating film in said trench.

136. (New) A method of fabricating a semiconductor integrated circuit device, as defined in claim 103, wherein by said step (g), a height of steps of said conductive film formed over said semiconductor substrate and of said conductive film formed over said isolating element is reduced.

137. (New) A method of fabricating a semiconductor integrated circuit device, as defined in claim 124, wherein by said step (h), a height of steps of said gate electrode formed over said semiconductor substrate and of said gate electrode formed over said isolating element is reduced.

138. (New) A method of fabricating a semiconductor integrated circuit device, as defined in claim 127, wherein by said step (g), a height of steps of said gate electrode formed over said semiconductor substrate and of said gate electrode formed over said isolating element is reduced.

139. (New) A method of fabricating a semiconductor integrated circuit device, as defined in claim 103, wherein a step is formed at an end of the isolating element, and a corresponding step is carried over to the conductive film formed on said step formed at the end of the isolating element.

140. (New) A method of fabricating a semiconductor integrated circuit device, as defined in claim 139, wherein in said removing the top of said conductive film a height of said corresponding step is reduced.

141. (New) A method of fabricating a semiconductor integrated circuit device, as defined in claim 124, wherein a step is formed at an end of the isolating element, and a corresponding step is carried over to the gate electrode formed on said step formed at the end of the isolating element.

142. (New) A method of fabricating a semiconductor integrated circuit device, as defined in claim 141, wherein in said removing the top of said gate electrode a height of said corresponding step is reduced.

143. (New) A method of fabricating a semiconductor integrated circuit device, as defined in claim 127, wherein a step is formed at an end of the isolating element, and a corresponding step is carried over to the gate electrode formed on said step formed at the end of the isolating element.

144. (New) A method of fabricating a semiconductor integrated circuit device, as defined in claim 143, wherein in said removing the top of said gate electrode a height of said corresponding step is reduced.